CSE460: VLSI Design Handout (Fall 2024)

## 

## Course Outcomes and Contents

| **Course Outcomes** | | **Course Contents** | |
| --- | --- | --- | --- |
| CO1 | Before Midterm | * Review of Digital Logic Design, * Logic design with CMOS, * CMOS DC Response | |
| After Midterm | * Delay and Power considerations in CMOS logic circuits | |
| CO2 | | * Finite State Machine design with logic gates | |
| CO3 | | * Fabrication and Layout design with stick diagram | |
| CO4 | | * Algorithms in Physical Design - Partitioning algorithm and Routing Algorithm | |

## Marks distribution

| **Theory/Lab** | **Assessment** | **Percentage** | **Total number of assessments** | **Number of assessment to be graded** |
| --- | --- | --- | --- | --- |
| Theory  (75%) | Attendance | **-** | - | 70% (90%+ for lab) or more to be eligible for Final Exam |
| Assignment | **10%** | 3~4 | Variable section wise |
| Quiz**\*** | **15%** | 3/4 (n) | Best 3 (n-1) |
| Midterm | **25%** | 1 | 1 |
| Final | **25%** | 1 | 1 |
| Lab  (25%) | Lab Assignment | **5%** | 2 | (70 (best) -30) Averaging |
| Lab Performance | **10%** | 5/6 (n) | Best (n-2) |
| Lab-test | **10%** | 1 | 1 |

**\***The last quiz (nth quiz) will be considered as make-up for any missed quiz (maximum of 1), whatever the reason. **No other make-up quizzes will be taken.**  
**Make-Up Lab Policy:** No make-up of lab will be considered without **valid reason.**

## 

## Semester Schedule Summary (tentative)

| **Exam** | **Time** | **Date** | **Syllabus\*** | **COs** |
| --- | --- | --- | --- | --- |
| **Quiz 1** | 3nd Week | [TBA] | Lecture 1-3 | *CO1* |
| **Quiz 2** | 5th Week | Lecture 8-10 | *CO2* |
| ***Midterm*** | ***6th Week*** | ***23 November, 2024*** | ***Lecture 1-10 (exc. 5-6)*** | *CO1, CO2* |
| **Quiz 3** | 10th Week | [TBA] | Lecture 12-15 | *CO3, CO4* |
| **Quiz 4** | 11th Week | Lecture 16- 17 | *CO1* |
| ***Final*** | ***14th Week*** | ***11 January, 2025*** | ***Lecture 11-20*** | *CO1, CO3, CO4* |

\*Follow [course timeline](#_4twyxbnafwi2)

## Theory Class Schedule

| **Section** | **Faculty** | **Day** | **Schedule** | **Room** | **Classes** |
| --- | --- | --- | --- | --- | --- |
| 1 | UPM | SAT, THU | 08:00 AM-09:20 AM | 09A-07C | 9 + 10 |
| 2 | KFP | SAT, THU | 09:30 AM-10:50 AM | 09A-07C | 9 + 10 |
| 3 | YAR | SAT, THU | 11:00 AM-12:20 PM | 09A-07C | 9 + 10 |
| 4 | PMD | SAT, THU | 12:30 PM-01:50 PM | 09A-07C | 9 + 10 |
| 5 | YAP | SAT, THU | 02:00 PM-03:20 PM | 09A-07C | 9 + 10 |
| 6 | UPM | SUN, TUE | 02:00 PM-03:20 PM | 09A-05C | 9 + 12 |
| 7 | THL | MON, WED | 03:30 PM-04:50 PM | 07H-26C | 9 + 9 |

## Lab Schedule and Status

| **Section** | **Faculty** | **Day** | **Schedule** | **Room** | **Lab Executed** |
| --- | --- | --- | --- | --- | --- |
| 1 | HAD, KFP | SUN | 08:00 AM-10:50 AM | 10G-33L | LAB1 (DSCH2) |
| 2 | HAD, AGS | SUN | 11:00 AM-01:50 PM | 10G-33L | LAB1 (DSCH2) |
| 3 | PMD, HAD | MON | 02:00 PM-04:50 PM | 12F-31L | **LAB1 (DSCH2)** |
| 4 | THL, SDU | TUE | 02:00 PM-04:50 PM | 12D-26L | LAB1 (DSCH2) |
| 5 | SDU, HAD | WED | 11:00 AM-01:50 PM | 12F-31L | **LAB1 (DSCH2)** |
| 6 | KFP, AGS | SAT | 02:00 PM-04:50 PM | 12F-31L | **LAB1 (DSCH2)** |
| 7 | SDU, YAP | THU | 08:00 AM-10:50 AM | 12F-31L | **LAB1 (DSCH2)** |

## 

# Course Team

## Theory Faculties

| **Initial** | **Name** | **BRACU Email** |
| --- | --- | --- |
| KFP | Kaniz Fatema Supti | kaniz.supti@bracu.ac.bd |
| PMD | Prithu Mahmud | prithu.mahmud@bracu.ac.bd |
| UPM | Tasnim Sobhan Upoma | tasnim.upoma@bracu.ac.bd |
| YAP | Yeasin Arafat Pritom | ext.yeasin.arafat@bracu.ac.bd |
| THL | Mohammad Tahsin Alam | tahsin.alam@bracu.ac.bd |

## Lab Faculties

| **Initial** | **Name** | **BRACU Email** |
| --- | --- | --- |
| HAD | Shadman Shahid | shadman.shahid@bracu.ac.bd |
| KFP | Kaniz Fatema Supti | kaniz.supti@bracu.ac.bd |
| PMD | Prithu Mahmud | prithu.mahmud@bracu.ac.bd |
| YAP | Yeasin Arafat Pritom | ext.yeasin.arafat@bracu.ac.bd |
| AGS | Aroni Ghosh | aroni.ghosh@bracu.ac.bd |
| THL | Mohammad Tahsin Alam | tahsin.alam@bracu.ac.bd |
| SDU | Shomen Kundu | shomen.kundu@bracu.ac.bd |
| UPM | Tasnim Sobhan Upoma | tasnim.upoma@bracu.ac.bd |

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# Course Resources

## Lab softwares

* **dsch2**

Download link: <https://drive.google.com/drive/folders/1xwzh8gbnfAvQBYRBd9xDs20lFbyK6SlJ?usp=sharing> (For experiments: 1)

* **Quartus**  
  Download link: <https://drive.google.com/drive/folders/1VVXijpn4d9LY4PS-Q_dAKXCU8q9xoESm?usp=sharing> (For experiments: 2, 3,4,5)
* **Microwind**

Download link: <https://drive.google.com/drive/folders/11xGLeyzWkfMV4nPgUqLjLi4eXAZVs7WM?usp=sharing> (For experiments: 6)

* Jupyter Notebook / Google Colab (For experiments: 7)

## Communication platform

CSE460 Summer ’24 Official Discord Server: <https://discord.gg/SKWWkFet>

## Textbooks

* **[Weste&Harris]** CMOS VLSI Design A Circuit and Systems Perspective 4e - Weste, Harris: <http://library.lol/main/51BD9C7E9E62DF12B1122C9B874DBFAC>   
  [*Solution manual is also available online*]
* **[Brown&Vranesic]** Fundamentals of Digital Logic with Verilog Design 3e - Stephen Brown, Zvonko Vranesic: <http://library.lol/main/7084609A715D3C56A468C66D66DD1019>   
  [*Solution manual is also available online*]
* **[Andrew,Jens,Igor&Jin]** VLSI Physical Design: From Graph Partitioning to Timing Closure 1e - Andrew B. Kahng, Jens Lienig, Igor L. Markov, Jin Hu: [https://theswissbay.ch/pdf/Gentoomen%20Library/Misc/Summerer%20-%20VLSI%20Physical%20Design.pdf](https://theswissbay.ch/pdf/Gentoomen%20Library/Misc/Springer%20-%20VLSI%20Physical%20Design.pdf)
* [Naveed A. Sherwani] Algorithms for VLSI Physical Design automation (third edition)

<https://drive.google.com/file/d/1zN8dcQeKMQdQj-ejm17JCRlWwx58VpfZ/view?usp=share_link>

* ***Chapter wise topic lists from the Books-*** <https://drive.google.com/file/d/1nVr_EWHiICuEubedRChEcz0Y9VqXNJEx/view?usp=share_link>

## **Practice problems sheet**

After watching/attending the lectures and reading the corresponding texts, try to solve the following problems:

**Week-wise Practice Problems:**[**CSE460: VLSI Design Practice Problems for Exam (Fall 2023)**](https://docs.google.com/document/d/13pAXmYC_q117fgEZyQRJ1OIQ7rcE9Q---lPXxtTwh1Y/edit?usp=sharing)

**Solution Manual for Practice Problems:** **[**[**Answer\_Sheet**](https://docs.google.com/document/d/1Y70yjc5wabp2q_O8CFXedObz3WR1xvE3tokb0NFTdUk/edit?usp=sharing)**]**

\*\*[*The problems are compiled from the corresponding reading sections’ solved example problems or exercises.*]

**\*\*The final questions in the exam will be conceptual & analytical (theoretical and problem-solving).**

# Course timeline

| **Week** | **Event** | **Details/Syllabus** | **Reference** | **Slide** | **BuX Video Link** |
| --- | --- | --- | --- | --- | --- |
| **1**  [Oct 22  -  Oct 24] | Theory: Week 1 Lecture 1 | Introduction to VLSI | [Weste&Harris] Chapter 1  1.1 A Brief History | [CSE460 Lecture 1.pptx](https://docs.google.com/presentation/d/1TRMNbH0eItqd7PTGwAfDic4RmG6WAGvU/edit?usp=sharing&ouid=115813789423266396797&rtpof=true&sd=true) | 1. [Course Content](https://www.youtube.com/watch?v=mJu9fpg3MbI)  2. [The transistor concept](https://www.youtube.com/watch?v=UAyXRaHNL1k)  3.[History and basic transistor](https://www.youtube.com/watch?v=BKh7z2kx6ec)  4.[MOSFETs: A closer look](https://www.youtube.com/watch?v=xgQmFFLcIsw)  5.[Moore's Law](https://www.youtube.com/watch?v=qeDwCbBLGY0)  6.[Design abstraction and methodologies](https://www.youtube.com/watch?v=5oXYlS-uYEI) |
| **2**  [Oct 26  -  Oct 31] | Theory: Week 2 Lecture 1 | - Review of digital electronics  - Logic gates in CMOS | [Brown&Vranesic]  Chapters 2, 4, 5  2.4 Logic Gates and Networks [Full, up to Functionally Equivalent Networks]  2.3 Boolean Algebra: Axioms of Boolean Algebra, Examples: 2.3, 2.4  4.1 Multiplexers [up to example 4.1(included)] 5.3 Gated D Latch [Full, 5.3.1 will be covered in future]  5.4.1 Master-Slave D Flip-flop [Full] | [CSE460 Lecture 2.pptx](https://docs.google.com/presentation/d/1zPy4aBam64ZhaGfzUzkoonMvlJ0N7npa/edit?usp=share_link&ouid=115813789423266396797&rtpof=true&sd=true) | 1.[Review of logic gates](https://www.youtube.com/watch?v=RcxuKJAIqg8)  2.[Logic function synthesis (SOP, POS, K-maps)](https://www.youtube.com/watch?v=hcCqpXwRtpA)  3.[Review of MUX](https://www.youtube.com/watch?v=g_piW_cVMg8)  4.[Review of Mux, Decoder and Encoder (optional)](https://www.youtube.com/watch?v=laWRIyPDOeI)  5.[Review of D latch](https://www.youtube.com/watch?v=GPSxuZvVPU4)  6.[Review of D flip-flop](https://www.youtube.com/watch?v=Dh_KKtuWgjI)  7.[Level triggered vs. Edge triggered](https://www.youtube.com/watch?v=dFNgRTbCTGU) |
| Theory: Week 2 Lecture 2 | Implementation of logic blocks and sequential elements in CMOS technology | [Weste&Harris] Chapter 1  1.3 MOS Transistors (full)  1.4 CMOS Logic (1.4.1-1.4.5) | [CSE460 Lecture 3.pptx](https://docs.google.com/presentation/d/1N1uknfiO9Prn3l7G0Fbk82ZM61qK_BWM/edit?usp=sharing&ouid=115813789423266396797&rtpof=true&sd=true) | 1. [460 L3 P1](https://www.youtube.com/watch?v=DcNluKKrmdI)  2. [nMOS and pMOS operation](https://www.youtube.com/watch?v=I84v0g4M4iU)  3. [CMOS logic gate general structure: part 1](https://www.youtube.com/watch?v=RICvIDHU0yk)  4.[CMOS logic gate general structure: part 2](https://www.youtube.com/watch?v=03UXvgaKYsk)  5.[Example 1](https://www.youtube.com/watch?v=YurhPT9l0Vo)  6.[Example 2](https://www.youtube.com/watch?v=xju8NFb-jT4)  7.[Example 3](https://www.youtube.com/watch?v=8bM7ltfNUjw) |
| **3**  [Nov 2  -  Nov 7] | **Lab:** Experiment 1 | CMOS Schematic Circuit Design in DSCH2 | [CSE 460 Experiment 1 (DSCH2).pdf](https://drive.google.com/file/d/1LlHInZL-pw-NQhwPbvH7VeobEh_XTBJr/view?usp=share_link) |  | 1.[CSE 460 Experiment 4 Part 1 : Introduction to DSCH2](https://www.youtube.com/watch?v=pqQqr5TT7to)  2.[CSE 460 Experiment 4 Part 2 : DSCH2 Example - CMOS Inverter](https://www.youtube.com/watch?v=Zo1nCareFJ8)  3.[CSE 460 Experiment 4 Part 3 : DSCH2 Example - F= AB+CD](https://www.youtube.com/watch?v=ZoMN5kF-sgQ)  4.[CSE 460 Experiment 4 Part 4 : DSCH2 Example - NAND gate](https://www.youtube.com/watch?v=wPnnReoL0D4)  5.[DSCH2 Example - D latch](https://www.youtube.com/watch?v=-HablBLtRcQ)  6.[DSCH2 Example D Flip Flop](https://www.youtube.com/watch?v=bHnZYKDDkr8) |
| Theory: Week 3 Lecture 1 | CMOS Implementation | [Weste&Harris] Chapter 1  1.4 CMOS Logic (1.4.6-1.4.9) | [CSE460 Lecture 4.ppt](https://docs.google.com/presentation/d/1G-0NHe5Ls1_YE9GFIKtRjWeMHeoY5eW1/edit?usp=sharing&ouid=115813789423266396797&rtpof=true&sd=true) | 1.[nMOS and pMOS as pass transistors](https://www.youtube.com/watch?v=l588g6kTwig)  2.[CMOS Transmission gates](https://www.youtube.com/watch?v=eR0RgGKGWTI)  3.[CMOS Tristate buffers and inverters](https://www.youtube.com/watch?v=1zSZ75jp3MQ)  4.[CMOS Multiplexers](https://www.youtube.com/watch?v=5NE5ESZMDuo)  5.[CMOS D Latch](https://www.youtube.com/watch?v=S-do28E3BlQ)  6.[CMOS D Flip-flop](https://www.youtube.com/watch?v=LzSno4vso0c) |
| Theory: Week 3 Lecture 2 | MOSFET Capacitance + DC response of CMOS inverter | [Weste&Harris] Chapter 2  2.3.1 Simple MOS capacitance models +  2.5 DC Transfer Characteristics  2.5.1 Static CMOS Inverter DC Characteristics  2.5.2 Beta Ratio Effects  2.5.4 Pass Transistor DC Characteristic | [CSE460 Lecture 5\_6\_CMOS\_Transistor\_Theory.pdf](https://drive.google.com/file/d/1SmoQXjSBWqLUofM_00zGASsiNsBzwg0z/view?usp=share_link)  **\*Lecture 5-6:** From slide 21 - 24  [CSE460 Lecture 7\_CMOS\_DC\_characteristics.pdf](https://drive.google.com/file/d/1n0MMZ_ps3lvkx8jTUySR0_xhG4Uv-R-2/view?usp=sharing) | 1.[Gate and diffusion capacitance](https://www.youtube.com/watch?v=opvHrOObotE)  2. [DC Response](https://www.youtube.com/watch?v=bPZWBu3dURU)  3.[CMOS Inverter DC Response Derivation](https://www.youtube.com/watch?v=a7DTGNqh5Hw)  4.[DC Response Practical Considerations](https://www.youtube.com/watch?v=Y2RGHQWCDLY) |
| **4**  [Nov 9  -  Nov 14] | **Lab**: Experiment 2  **[ Lab assignment 1 to be provided ]** | Introduction to Verilog; Verilog Design Part 1 (combinational logic) | [Altera Quartus Manual](https://docs.google.com/document/d/12DPaHPxBLSndnKpRMMhBJ2kLdWc9HjUtE8z0Jlxwpv8/edit?usp=drive_link)[CSE 460 Experiment 2 (Verilog 1).pdf](https://drive.google.com/file/d/15TstnXw8nRI87uav_TKqzagFG7sEo6sC/view?usp=drive_link) | [CSE460 Lab-2 Presentation.pptx](https://docs.google.com/presentation/d/1M6cfea0_wbvscZWDj9OJni5XJkSJ4Lj2/edit?usp=drive_link&ouid=115813789423266396797&rtpof=true&sd=true) |  |
| Theory: Week 4 Lecture 1 | Introduction to system design using finite state machines | [Brown&Vranesic]  Chapter 6  6.1 Basic Design Steps  [Brown&Vranesic]  Chapter 6  Example 6.1 [full] | [CSE460 Lecture 6\_KMAP(Spring23\_AHB).pptx](https://docs.google.com/presentation/d/1rBaD0OW4CDg4Q_NmGBhgsrZuS-PIsMdm/edit?usp=sharing&ouid=115813789423266396797&rtpof=true&sd=true)[CSE460 Lecture 6\_FSM1 (Spring23\_AHB).pptx](https://docs.google.com/presentation/d/1slh1TLwEzVR_HOuXrYQVzgTxGMeWq0NI/edit?usp=sharing&ouid=115813789423266396797&rtpof=true&sd=true) | [D-Flip Flop and K-Map review](https://youtu.be/EMchUnRxc80?si=_ZVWfvfogxfpOmnf)  [FSM Examples Mix - Fall23](https://youtu.be/aeBzssniUto?si=bnPuoEa21ahL1gX7)  [**FSM Introduction + K-Map**](https://youtu.be/1FCOWhWq4oE?si=-Tqxei1uynLe4D6y) |
| Theory: Week 4 Lecture 2 | System design using moore and mealy type finite state machines (FSM1) | [CSE460 Lecture 9 (Spring23\_AHB).pptx](https://docs.google.com/presentation/d/1lW-zMkgGXL38U_zhaSTW8AmhnudnyRBT/edit?usp=sharing&ouid=115813789423266396797&rtpof=true&sd=true) | [Theory Lecture 8.2 | FSM - Moore](https://youtu.be/RJKgKpzywhA?si=60KhSZtnCBsp3lm8) |
| **5**  [Nov 16  -  Nov 21] | **Lab**: Experiment 3 | Verilog Design Part 2 (sequential logic) | [CSE 460 Experiment 3 (Verilog 2).pdf](https://drive.google.com/file/d/1Bmh3zyutPQ6jpDI_ik0asByFQcqAHpNb/view?usp=drive_link) | [CSE460 Lab-3 Presentation.pptx](https://docs.google.com/presentation/d/1haB4fPeXZgcuzeLXl-glJWZsAxbK_KNo/edit?usp=drive_link&ouid=115813789423266396797&rtpof=true&sd=true) |  |
| Theory: Week 6 Lecture 1 | System design using moore and mealy type finite state machines (FSM2) | [Brown&Vranesic] Chapter 6  Section 6.2, 6.2.1 [Full], 6.3 Mealy State Model [full]  Example 6.2, 6.4 | [CSE460 Lecture 8\_FSM2 (Spring23\_AHB).pptx](https://docs.google.com/presentation/d/1nohY9BPaAhwWuOGFxcXbjb5aaw0VEyvD/edit?usp=sharing&ouid=115813789423266396797&rtpof=true&sd=true) | [Theory Lecture 9 | FSM - Encoding Schemes, Mealy Type](https://youtu.be/ghA6-XwdgXE?si=No5trN_dvHKjdewM)  [Register Data Swap](https://youtu.be/aFQMPnvoowk?si=uOcLmmVWdBZ9EN96)  [Some Real FSMs](https://youtu.be/7ijUUrWh_vw?si=0kbn4vNPGGEuz1GQ) |
| **Theory** | Reserved | | |  |
| **6** | **Midterm exam** | **Lecture 1 - Lecture 10 (Excluding Lecture 5-6)** | | |  |
| **7**  [Dec 1  -  Dec 5] | **Lab**: Experiment 4  **[ Lab assignment 1 Submission Deadline ]** | Verilog Design Part 3 (FSMs) |  | [CSE460 Lab-4 FSM.pptx](https://docs.google.com/presentation/d/1z70yL7-QMCCCHnpIhNbjGTbtFoyf9JRO/edit?usp=drive_link&ouid=114642630939738632786&rtpof=true&sd=true) |  |
| Theory: Week 7 Lecture 1 | Fabrication of CMOS devices | [Weste&Harris] Chapter 1  1.5 CMOS Fabrication and Layout (1.5.1-1.5.3) | [CSE460 Lecture 11\_Fabrication(BRH).ppt](https://docs.google.com/presentation/d/14LGJ-de2Ftr_JTw5nhHFtldqnn1Csp3F/edit?usp=sharing&ouid=115813789423266396797&rtpof=true&sd=true) | [Theory Lecture 11 | Fabrication - 10 Steps Process](https://youtu.be/FsUHuS9DMDs?si=-4stPmpIjK_rHTnr) |
| Theory: Week 7 Lecture 2 | Layouts and stick diagrams | [Weste&Harris] Chapter 1  1.5.5 Stick Diagrams (Full + Example 3) | [CSE460 Lecture 12\_layout\_stick diagram.ppt](https://docs.google.com/presentation/d/1n2drcTwifNHK3-ySBc71YnAM3Bre0_ky/edit?usp=sharing&ouid=115813789423266396797&rtpof=true&sd=true)  [CSE460 Lecture 12\_stick diagram\_examples [V2].pptx](https://docs.google.com/presentation/d/1MlkTQ5sAmpNXdJdKdJUsroVamppV2CCw/edit?usp=share_link&ouid=115813789423266396797&rtpof=true&sd=true) | [Theory Lecture 12 | Stick Diagram](https://youtu.be/75WkfIUpYdw?si=A4ECyVpVCB5Oz2uN) |
| **8**  [Dec 7  -  Dec 12] | **Lab**: Experiment 5  **[ Lab assignment 2 to be provided ]** | Verilog Design Part 4 (FSMs) |  | [CSE460 Lab-5 Vending-Machine Fall 22.pptx](https://docs.google.com/presentation/d/1YN0I5-9bX2nfjsKVuo4EAcYnZXcZ8OdH/edit?usp=drive_link&ouid=115813789423266396797&rtpof=true&sd=true) |  |
| Theory: Week 8 Lecture 1 | 1. Physical Design |  | [CSE460 Lecture 13\_physical\_design\_and\_KL\_algorithm.pptx](https://docs.google.com/presentation/d/1wg9JXs6p97SNZ2ntHeyXUYbVeI4eLyMA/edit?usp=share_link&ouid=115813789423266396797&rtpof=true&sd=true) | [Theory Lecture 13+14 | Physical Design](https://youtu.be/IAjcBr2G6jM?si=hT6KpzktyrH3YxKI) |
| Theory: Week 8 Lecture 2 | Physical Design (algorithm 1) | Video URL: | [CSE460 Lecture 13\_physical\_design\_and\_KL\_algorithm.pptx](https://docs.google.com/presentation/d/1wg9JXs6p97SNZ2ntHeyXUYbVeI4eLyMA/edit?usp=share_link&ouid=115813789423266396797&rtpof=true&sd=true) |  |
| **9**  [Dec 14  -  Dec 19]  Dec 16  (Sun) | **Lab** **Test** | Experiment 1 - Experiment 3  [CSE 460 Experiment 4 (Verilog 3) Fall22 [AHB].pdf](https://drive.google.com/file/d/1uSPv6hfsWfRejUGu5sTkdc9vg9GGXaPB/view?usp=drive_link)  [CSE460 Lab-4 FSM.pptx](https://docs.google.com/presentation/d/1z70yL7-QMCCCHnpIhNbjGTbtFoyf9JRO/edit?usp=drive_link&ouid=115813789423266396797&rtpof=true&sd=true) | | |  |
| Theory: Week 9 Lecture 1 | Physical Design (algorithm 2) | Lecture note | [CSE460 Lecture 15+16\_Routing\_Algorithm\_Updated](https://docs.google.com/presentation/d/1QFM6YQi6MhdE6aaVADyulboH-_-wPiGat-qrf8PLf6k/edit?usp=sharing) | [Theory Lecture 15+16 | Lee's Maze Algorithm](https://youtu.be/hCjOC6KqEmY?si=SPlwHaz_F2Xq0oz-) |
| Theory: Week 9 Lecture 2 | Physical Design (algorithm 2) | Lecture note | [CSE460 Lecture 15+16\_Routing\_Algorithm\_Updated](https://docs.google.com/presentation/d/1QFM6YQi6MhdE6aaVADyulboH-_-wPiGat-qrf8PLf6k/edit?usp=sharing) |  |
| **10**  [Dec 21  -  Dec 24]  Dec 25, 26  (Wed, Thurs) | **Lab**: Experiment 6 | CMOS Layout Design in Microwind | [CSE 460 Experiment 6+7 (MW2).pdf](https://drive.google.com/file/d/1n5puFglr1iPv8I2DY6DPmqcXghQV6Zth/view?usp=drive_link) |  |  |
| Theory: Week 10 Lecture 1 | Delay in CMOS circuits(Part1) | [Weste&Harris] Chapter 4  4.2 Transient Response  4.3 RC Delay Model  4.3.1 Effective Resistance  4.3.2 Gate and Diffusion Capacitance  4.3.3 Equivalent RC Circuits | [CSE460 Lecture 15+16\_Delay.pdf](https://drive.google.com/file/d/1kgP0T7V_K2YiMsMU6eq3pf-VW1OLOxdL/view?usp=share_link) | [Theory Lecture 17 | Delay - Basics](https://youtu.be/nbIIeI6j4_0?si=ub3bCyk6BQlQhPjv)  [NAND-2 Delay](https://youtu.be/IryulQSc_9o?si=36FVYZC7EujNTzCW) |
| Theory: Week 10 Lecture 2 | Delay in CMOS circuits(Part2) | [Weste&Harris] Chapter 4  4.3.5 Elmore Delay  Example 4.3, 4.4, 4.5, 4.6, 4.7, 4.8, 4.9 | [CSE460 Lecture 15+16\_Delay.pdf](https://drive.google.com/file/d/1kgP0T7V_K2YiMsMU6eq3pf-VW1OLOxdL/view?usp=share_link) | [Theory Lecture 18 | Delay - Example (NAND3)](https://youtu.be/KcvJXb5Agwo?si=gfSmLl0N1-1NpE7m) |
| **11**  [Dec 28  -  Jan 2]  Jan 1  (Wed) | **Lab**: Experiment 7 | KL Algorithm implementation using Python | TBA |  |  |
| Theory: Week 11 Lecture 1 | Power in CMOS circuits | [Weste&Harris] Chapter 5  5.1.1 Definitions  5.1.2 Examples  5.1.3 Sources of Power Dissipation  Example 5.1 | [CSE460 Lecture 17+18\_POWER (Reference Slide).pdf](https://drive.google.com/file/d/1uNCtjtASlo06gK_C_05BaKY0QhVuEFov/view?usp=sharing)  [CSE460 Lecture 17+18\_POWER (buX Lecture Note).pdf](https://drive.google.com/file/d/1e1oFcTmx-ihGkyzYQVjjkPQrYtGsoYFY/view?usp=share_link) | [Theory Lecture 19+20 | Power](https://youtu.be/sshD6bp0iqo?si=UsCnCZD1zltVlbKn) |
| Theory: Week 11 Lecture 2 | Power in CMOS circuits (Continued) | [CSE460 Lecture 17+18\_POWER (Reference Slide).pdf](https://drive.google.com/file/d/1uNCtjtASlo06gK_C_05BaKY0QhVuEFov/view?usp=sharing) |  |
| **12**  [Jan 4  -  Jan 9] | **Lab: No lab [ Lab assignment 2 Submission Deadline ]** | | | |  |
| Theory | Reserved | | |  |
| **13**  [Jan 10  -  Jan 18] | **Final exam** | **Lecture 11 - Lecture 20** | | |  |

# Course contents

**Detailed List of Topics**

1. **Week 1**

* Introduction to VLSI, history, timeline. Moore’s law.

1. **Week 2**

* Review of digital logic design. Complete VLSI flow (top down / bottom up)
* Logic circuit families: n-MOS, p-MOS, pseudo n-MOS and CMOS technologies. Introduction to CMOS logic. Pull-up and pull-down networks, implementation using series and parallel MOSFETs.

1. **Week 3**

* Combinational logic circuit design using CMOS. Complex gate design using CMOS such as And-Or-Invert or Or-And-Invert. Implementation of different circuit elements like basic gates.
* Multiplexers, encoder, latch, flip-flops using CMOS
* DC Response of CMOS gates. Pass transistors. Logic levels and noise margins. DC transfer characteristics.

1. **Week 4**

* FSM Introduction
* FSM moore and mealy type machines

1. **Week 5**

* System design using moore and mealy type finite state machines
* Different hardware implementation techniques

1. **Week 6**

* Midterm week

1. **Week 8**

* CMOS Fabrication: Inverter cross-section and layout analysis.
* Layout
* Masks. Stick diagrams and area estimation. (Eulerian path. Complex examples)

1. **Week 9, 10**

* Physical design: floorplanning, partitioning, routing, clock tree synthesis.
* KL algorithm for partitioning.
* Lee’s maze algorithm for global routing

1. **Week 11**

* Transient response of CMOS gates. Delay definitions: rise time, fall time, propagation delay and contamination delay, RC delay model. Effective resistance. MOS Capacitance.
* Elmore delay. Parasitic and effort delay. Fan-in and fan-out. Layout comparisons

1. **Week 12**

* CMOS Power: Instantaneous and Average power, Energy. Power in circuit elements analysis (R, C, DC Supply). Switching waveforms of an inverter. Static power and Dynamic power. Activity factor. Power reduction techniques: Clock gating, Power gating, Dynamic voltage scaling.